PhysicsByAaryan

CSIR NET . GATE . JEST . BARC - Physics

Flip flops/Counters/Registers/microcontroller etc. - CSIR NET Physics PYQs

Electronics . All PYQs (2015-2025) with answer key

11 questions . Answer key included

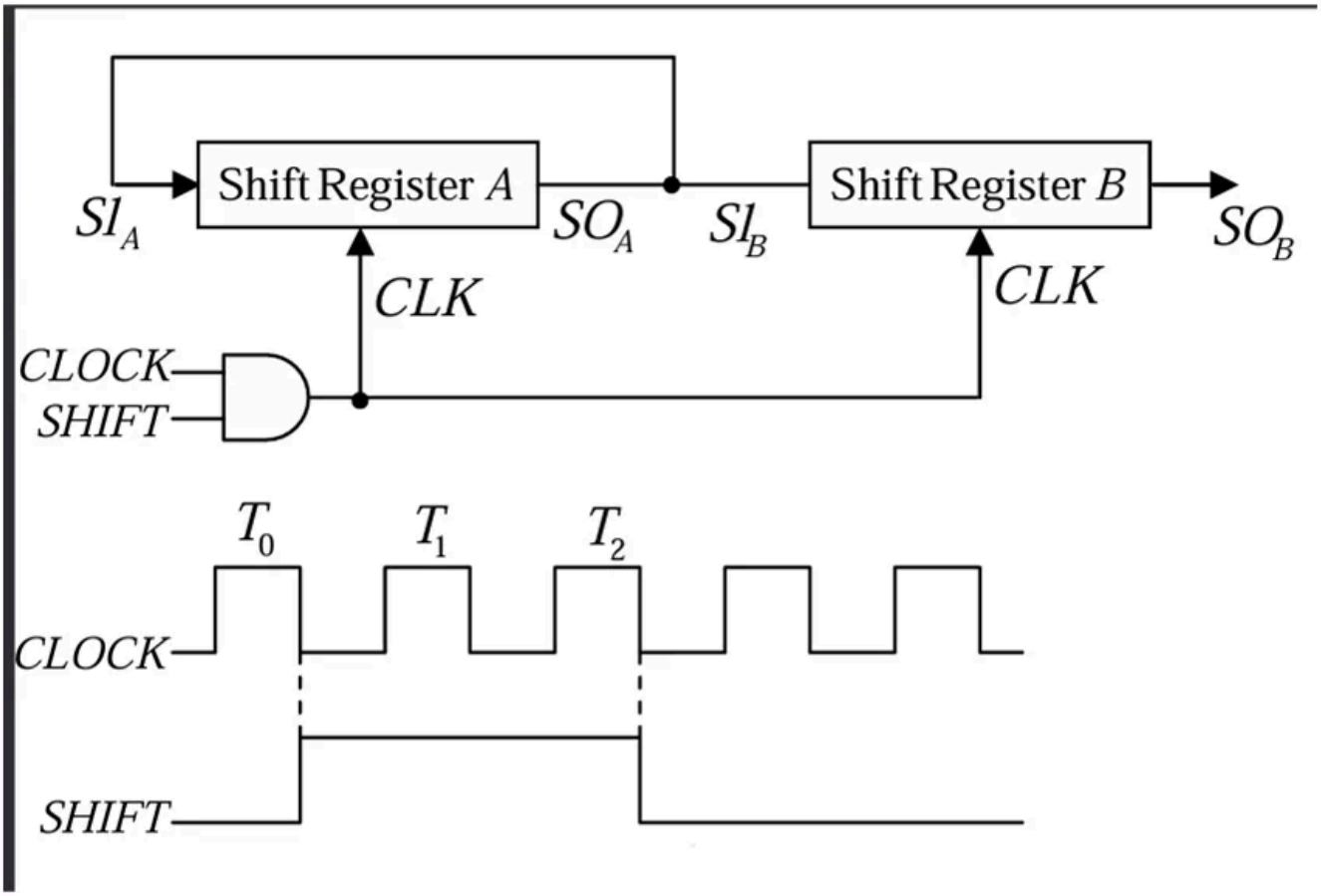
www.physicsbyaaryan.com . www.csirnetphysics.com
Contact: 9501976811

Q1. [Dec 2015] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2015 Dec	3.5 M

In the schematic figure given below the initial values of 4 bit shift registers A and B are 1011 and 0010 respectively The values at SO_A. and SO_B after the pulse T_2 are respectively.



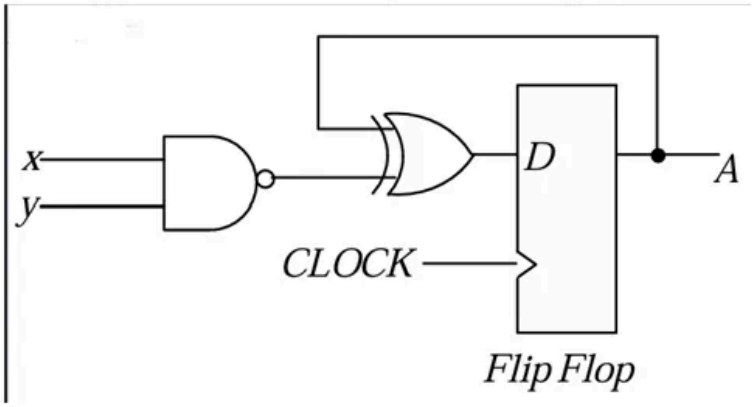
1. 1110 and 1001
2. 1101 and 1001
3. 1101 and 1100
4. 1110 and 1100

Q2. [Dec 2015] . 5.0 marks

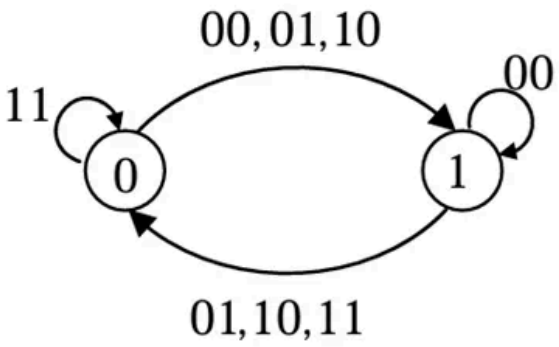
Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2015 Dec	5 M

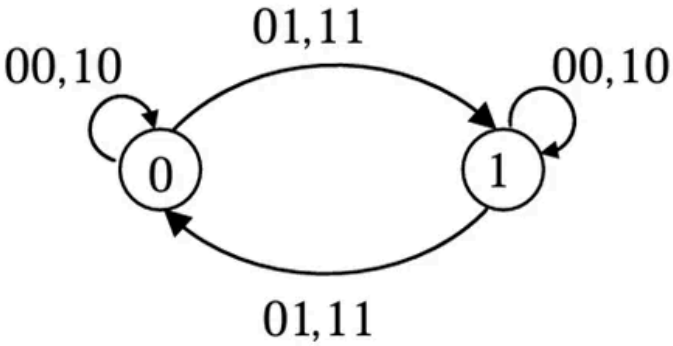
The state diagram corresponding to the following circuit is



1.



2.



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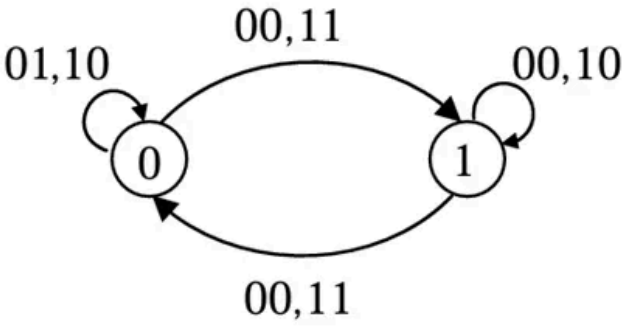
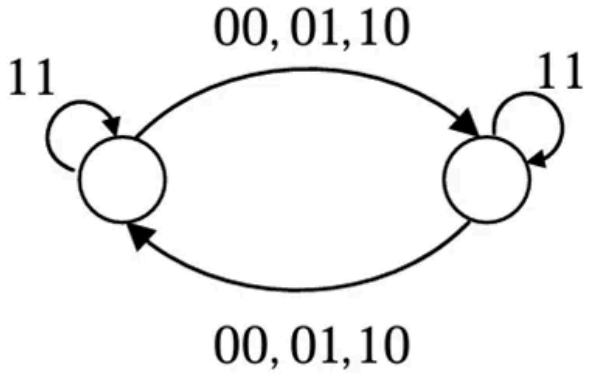


4.

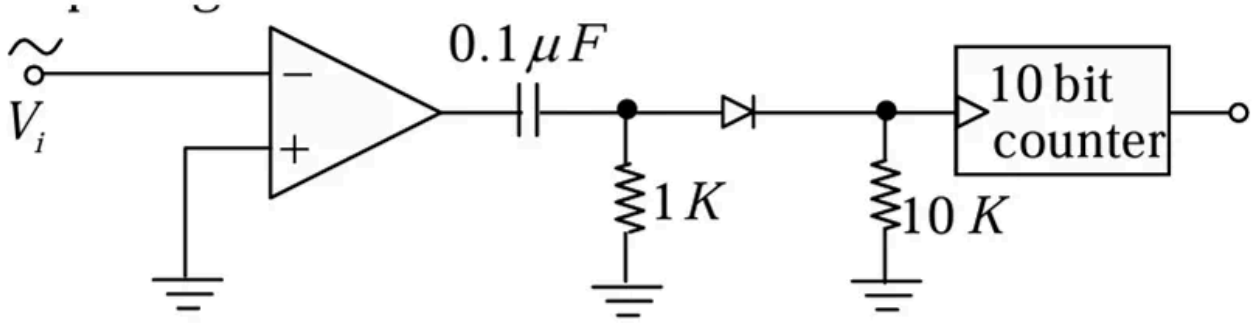


Q3. [Dec 2015] . 5.0 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2015 Dec	5 M

A sinusoidal signal of peak to peak amplitude 1 V and unknown time period is input to the following circuit for 5 seconds duration. If the counter measures a value $(3E8)_H$ in hexadecimal then the time period of the input signal is



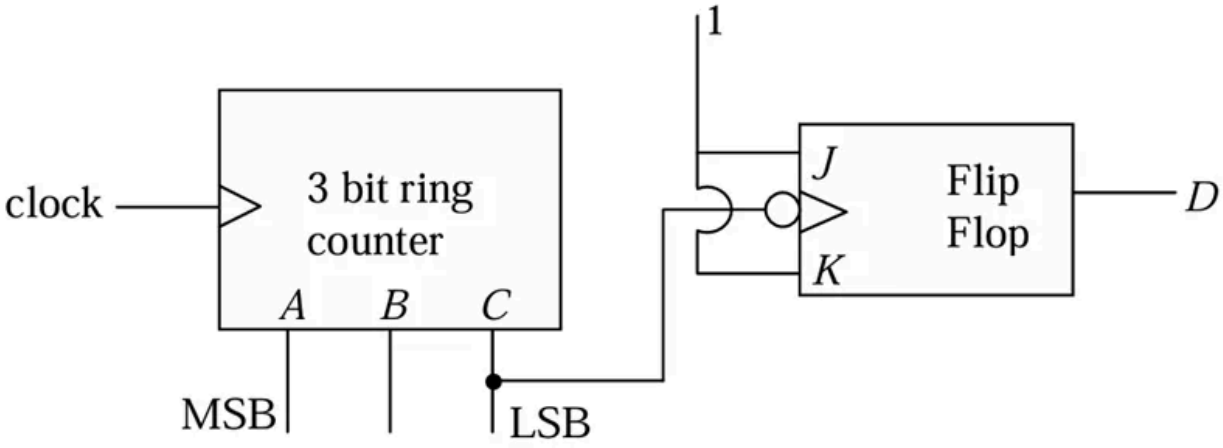
1. $2.5ms$
2. $4ms$
3. 10 ms
4. $5ms$

Q4. [June 2015] . 5.0 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2015 June	5 M

For the logic circuit given below, the decimal count sequence and the modulus of the circuit corresponding to A B C D are



1. $8 \rightarrow 4 \rightarrow 2 \rightarrow 1 \rightarrow 9 \rightarrow 5(mod6)$
2. $8 \rightarrow 4 \rightarrow 2 \rightarrow 9 \rightarrow 5 \rightarrow 3(mod6)$
3. $2 \rightarrow 5 \rightarrow 9 \rightarrow 1 \rightarrow 3(mod5)$
4. $8 \rightarrow 5 \rightarrow 1 \rightarrow 3 \rightarrow 7(\mathrm{mod}5)$

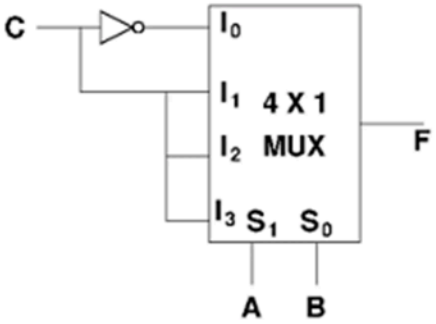
Q5. [Dec 2016] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

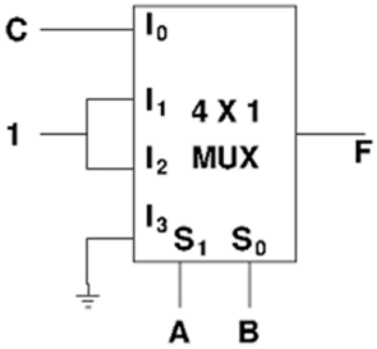
CSIR NET	2016 Dec	3.5M

Which of the following circuits implements the Boolean function $F(A,B,C) = \sum(1,2,4,6)$?

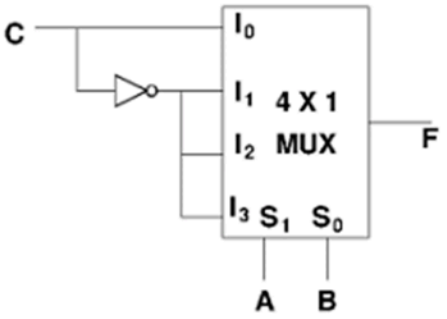
1.



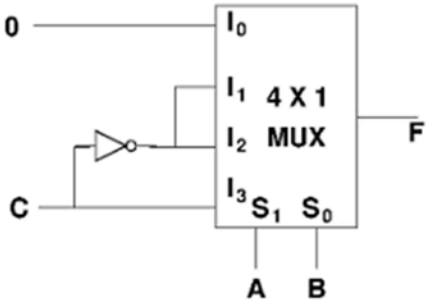
3.



2.



4.



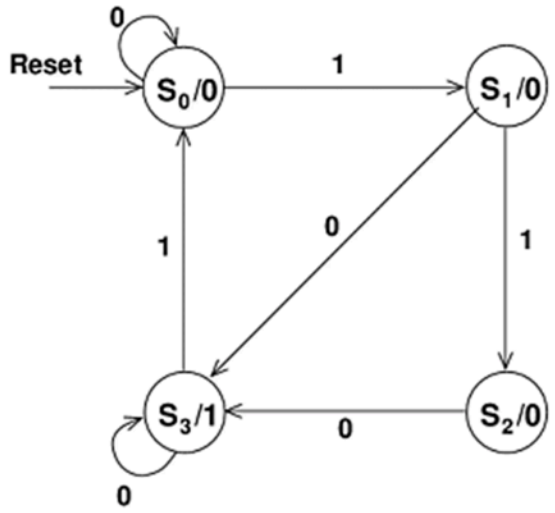
Q6. [June 2016] . 5.0 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

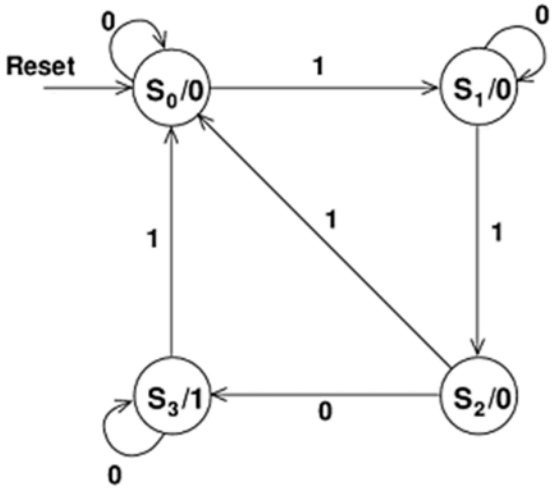
CSIR NET	2016 June	5M

The state diagram that detects three or more consecutive 1's in a serial bit stream is

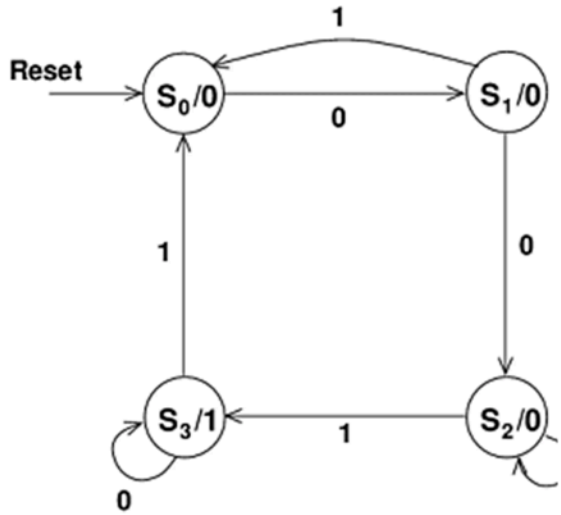
1.



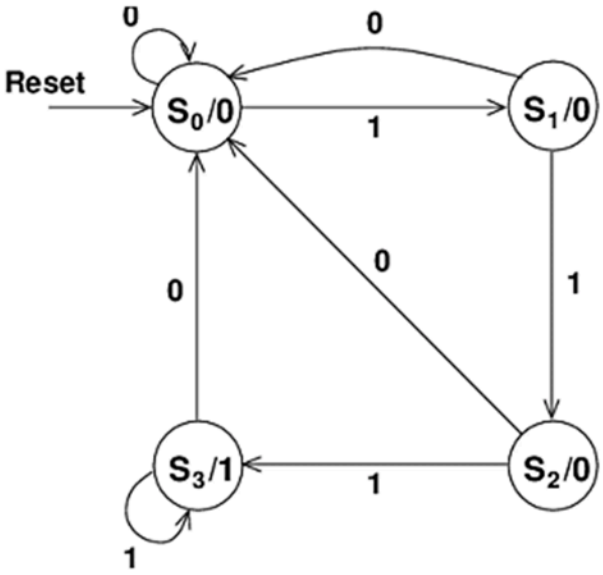
3.



2.



4.

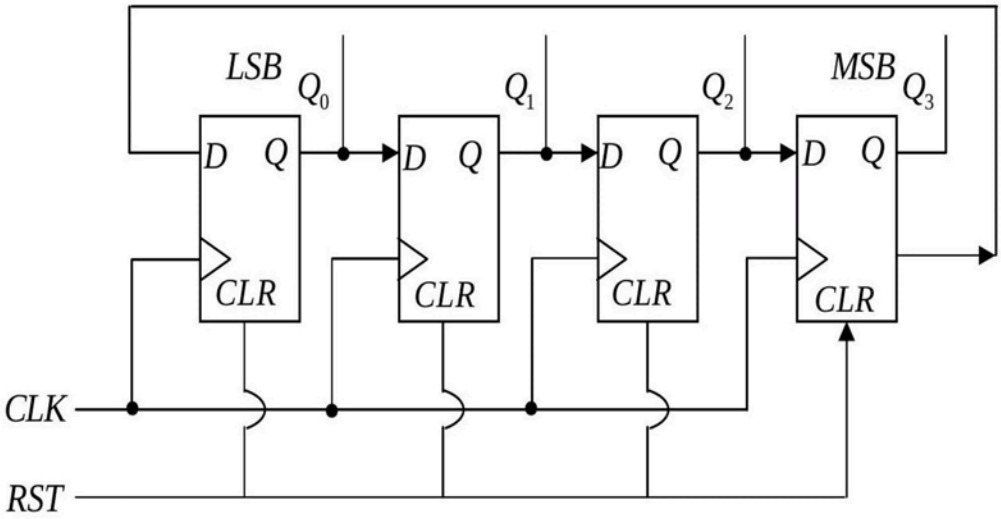


Q7. [Dec 2017] . 5.0 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2017 Dec	5M

The circuit below comprises of D-flip flops. The output is taken from Q_3, Q_2, Q_1 and Q_0 as shown in the figure.



The binary number given by the string Q_3, Q_2, Q_1Q_0 changes for every clock pulse that is applied to the CLK input. If the output is initialized at 0000 , the corresponding sequence of decimal numbers that repeats itself, is

1. 3,2,1,0
2. 1,3,7,14,12,8
3. 1,3,7,15,12,14,0
4. 1,3,7,15,14,12,8,0

Q8. [June 2017] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2017 June	3.5M

A 2×4 decoder with an enable input can function as a

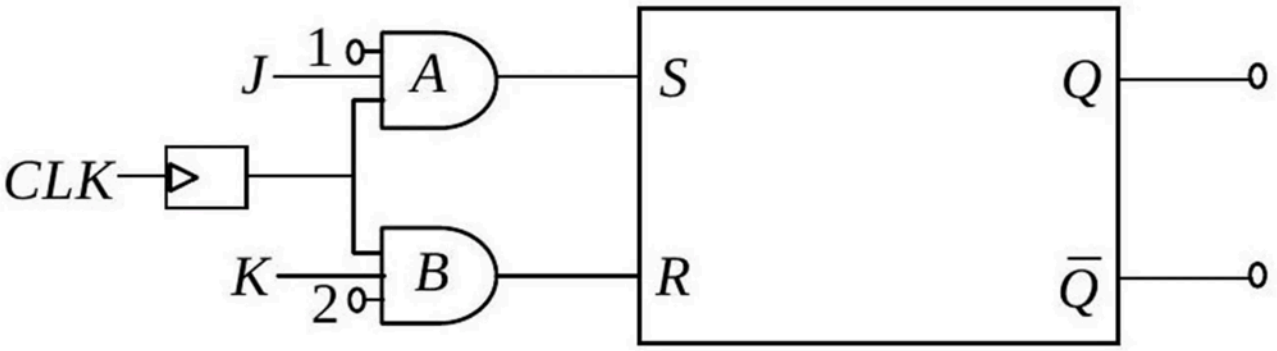
1. 4×1 multiplexer
2. 1×4 demultiplexer
3. 4×2 encoder
4. 4×2 priority encoder

Q9. [Dec 2018] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2018 Dec	3.5M

Consider the following circuit, consisting of an RS flip-flop and two AND gates.



Which of the following connections will allow the entire circuit to act as a JK flip-flop?

1. connect Q to pin 1 and $\bar{Q}$ to pin 2
2. connect Q to pin 2 and $\bar{Q}$ to pin 1
3. connect Q to K input and $\bar{Q}$ to J input
4. connect Q to J input and $\bar{Q}$ to K input

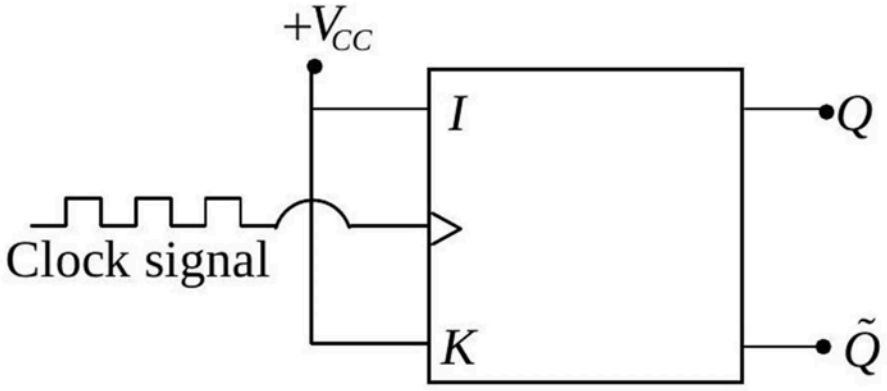
Q10. [June 2018] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2018 June	3.5M

In the following JK flip-flop circuit, J and K inputs are tied together to $+V_{CC}$. If the input is a clock signal of frequency f, the frequency of the output Q is

1. f
2. $2f$
3. $4f$
4. $\frac{f}{2}$

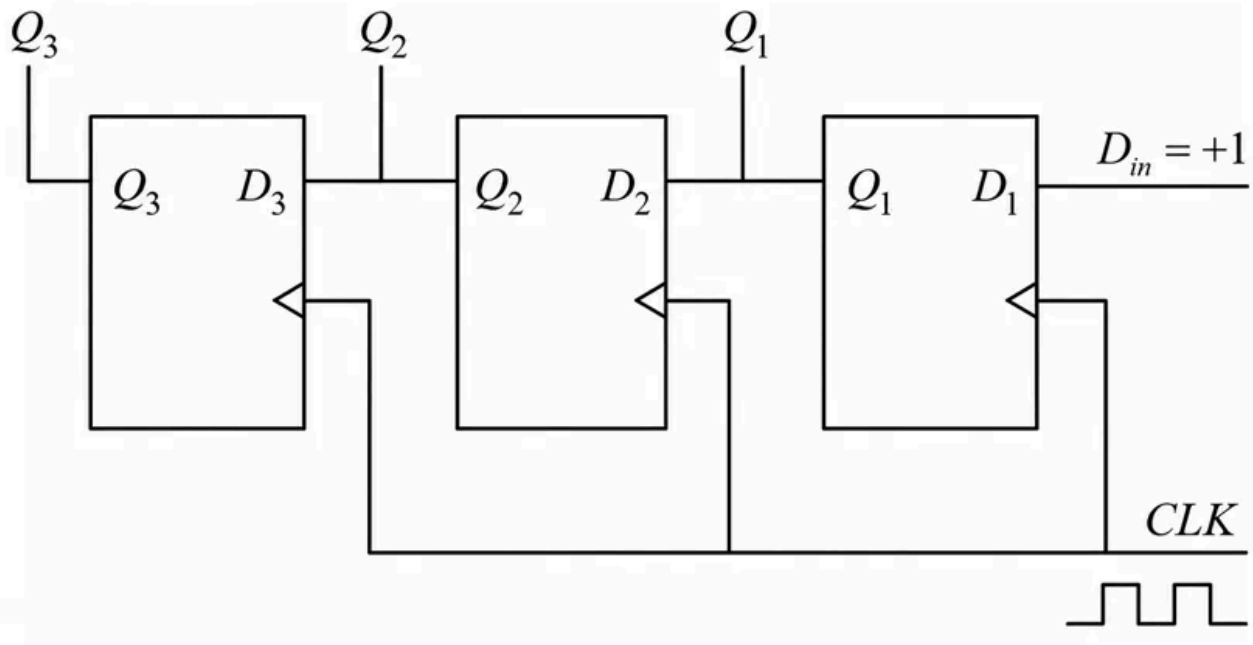


Q11. [June 2020] . 3.5 marks

Electronics > Flip flops/Counters/Registers/microcontroller etc.

CSIR NET	2020 June	3.5M

In the 3 -bit register shown below, Q_1 and Q_3 are the least and the most significant bits of the output, respectively.



If Q_1, Q_2 and Q_3 are set to zero initially, then the output after the arrival of the second falling clock (CLK) edge is

1. 001
2. 100
3. 011
4. 110

Answer Key

11 questions . Subject and topic for quick revision

Q. No	Subject	Topic	Answer
Q1	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q2	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q3	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q4	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**2**
Q5	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**2**
Q6	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q7	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q8	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**2**
Q9	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**2**
Q10	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**4**
Q11	Electronics	Flip flops/Counters/Registers/microcontroller etc.	**3**

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