PhysicsByAaryan

CSIR NET . GATE . JEST . BARC - Physics

Digital Electronics - CSIR NET Physics PYQs

Electronics . All PYQs (2015-2025) with answer key

16 questions . Answer key included

www.physicsbyaaryan.com . www.csirnetphysics.com
Contact: 9501976811

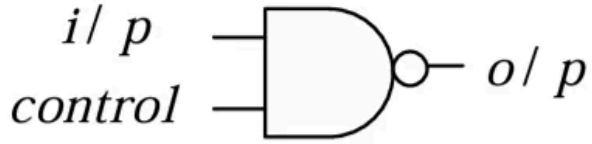
Q1. [June 2015] . 3.5 marks

Electronics > Digital Electronics

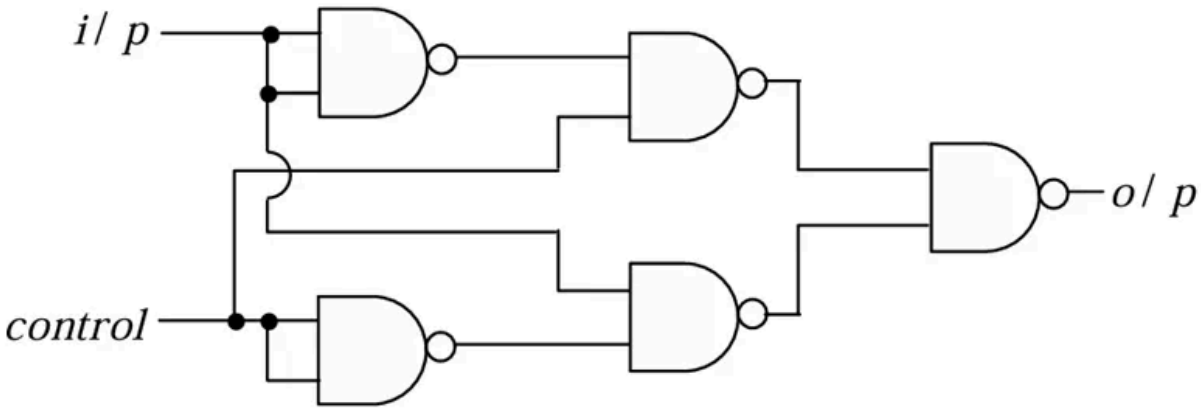
CSIR NET	2015 June	3.5 M

Which of the following circuits behaves a control invertor?

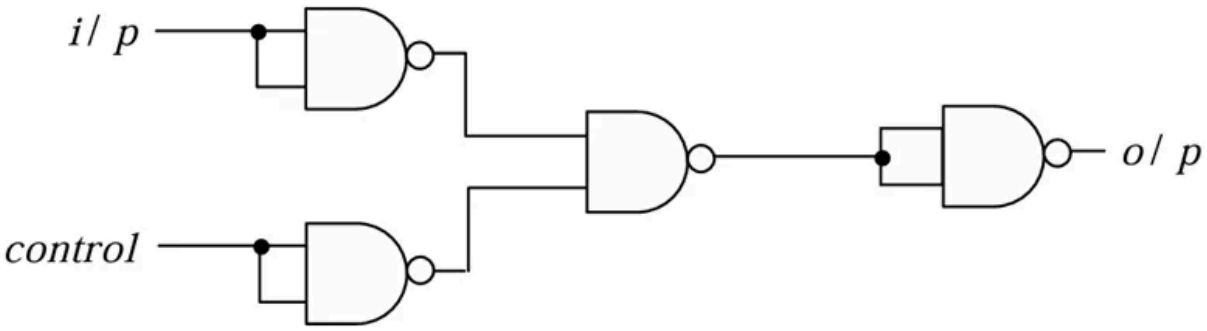
1.



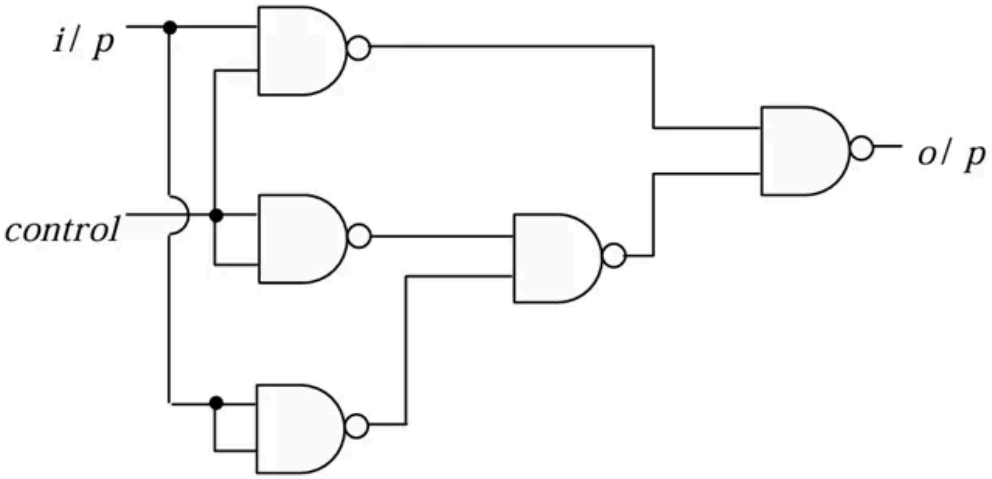
2.



3.



4.



Q2. [June 2016] . 3.5 marks

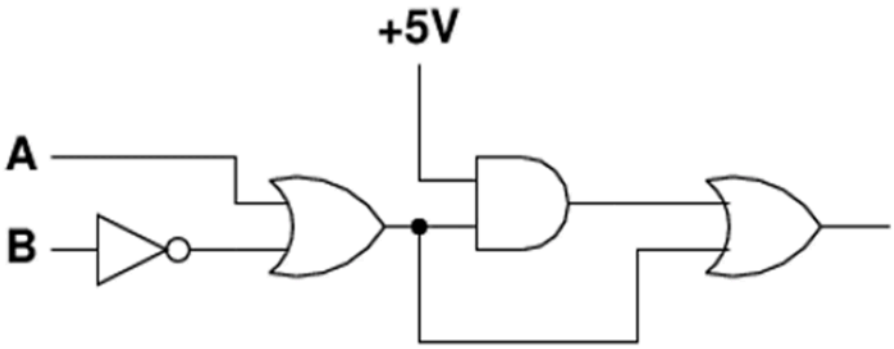
Electronics > Digital Electronics

CSIR NET	2016 June	3.5M

In the schematic figure given below, assume that the propagation delay of each logic gate is t_{gate} .

The propagation delay of the circuit will be maximum when the logic inputs A and B make the transition

1. $(0,1) \rightarrow (1,1)$
2. $(1,1) \rightarrow (0,1)$
3. $(0,0) \rightarrow (1,1)$
4. $(0,0) \rightarrow (0,1)$



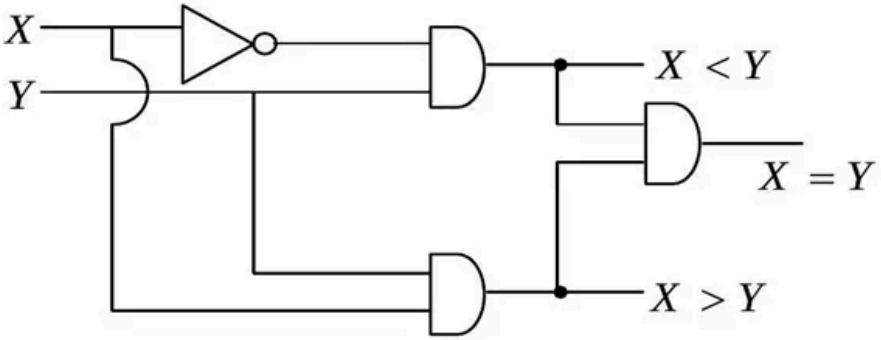
Q3. [June 2017] . 5.0 marks

Electronics > Digital Electronics

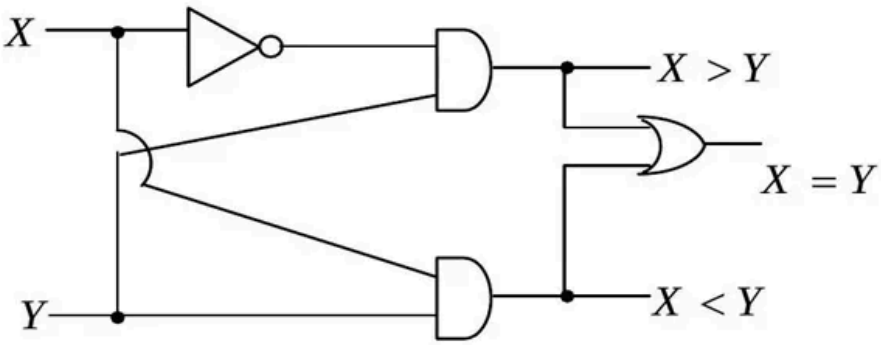
CSIR NET	2017 June	5M

In the figures below, X and Y are one bit inputs. The circuit which corresponds to a one bit comparator is

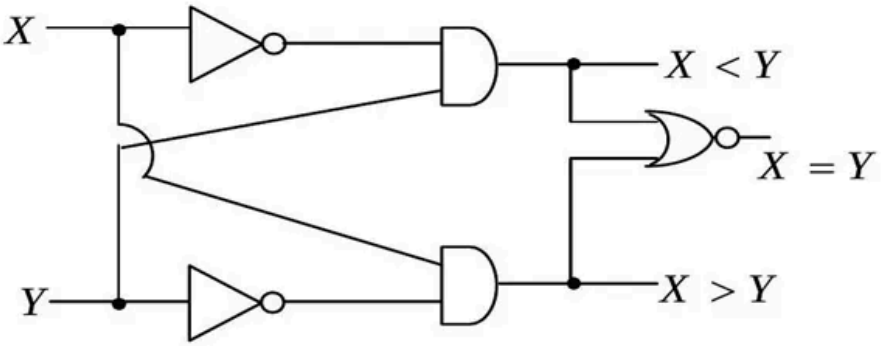
1.



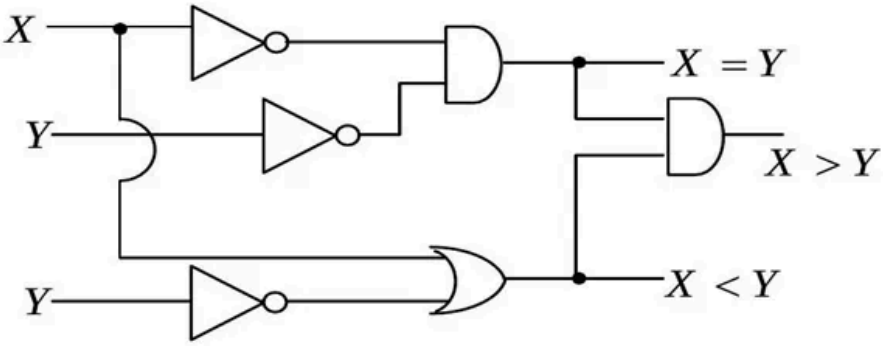
2.



3.



4.



Q4. [Dec 2018] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2018 Dec	3.5M

The truth table below gives the value $Y(A, B, C)$ where A, B and C are binary variables. The output Y can be represented by

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	1	0	0
1	1	1	1

1. $Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}C + AB\bar{C}$
2. $Y = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$
3. $Y = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}C + ABC$
4. $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + AB\bar{C}$

Q5. [June 2018] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2018 June	3.5M

Which of the following gates can be used as a parity checker?

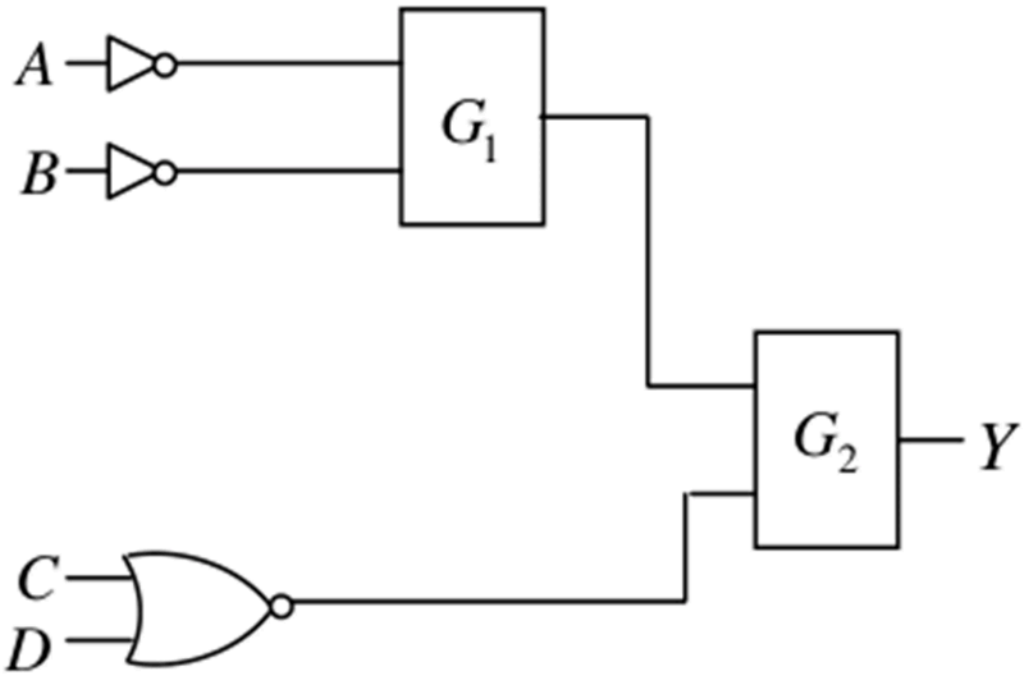
1. an OR gate
2. a NOR gate
3. an exclusive OR (XOR) gate
4. an AND gate

Q6. [June 2019] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2019 June	3.5M

Let Y denote the output in the following logical Circuit.



If $Y = AB + \bar{C}D$, the gates G_1 and G_2 must, respectively, be

1. OR and NAND
2. NOR and OR
3. AND and NAND
4. NAND and OR

Q7. [June 2020] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2020 June	3.5M

The Boolean equation $Y = \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C$ is to be implemented using only two-input NAND gates. The minimum number of gates required is

1. 3
2. 4
3. 5
4. 6

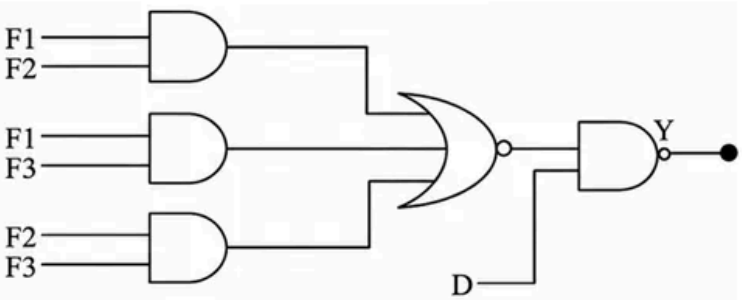
Q8. [June 2021] . 3.5 marks

Electronics > Digital Electronics

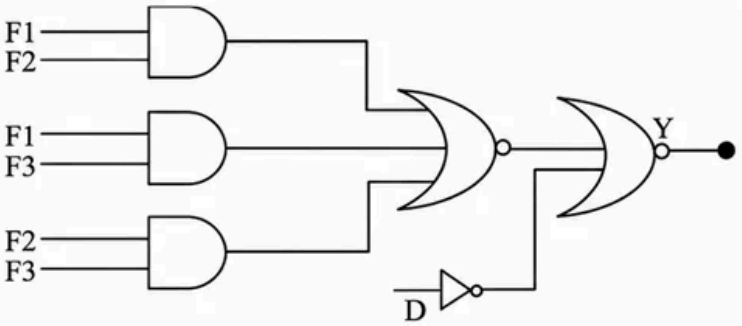
CSIR NET	2021 June	3.5M

The door of an X-ray machine room is fitted with a sensor D (0 is open and 1 is closed). It is also equipped with three fire sensors F_1, F_2 and F_3 (each is 0 when disabled and 1 when enabled). The X-ray machine can operate only if the door is closed and at least 2 fire sensors are enabled. The logic circuit to ensure that the machine can be operated is

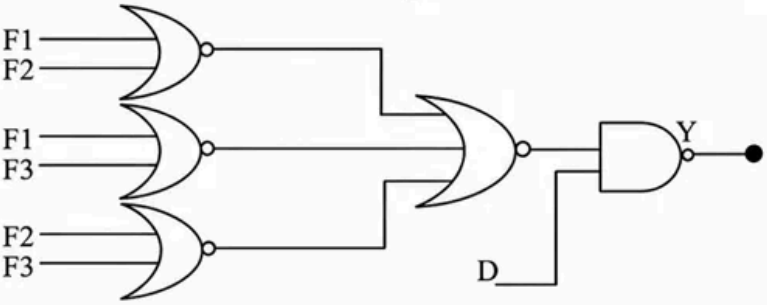
1.



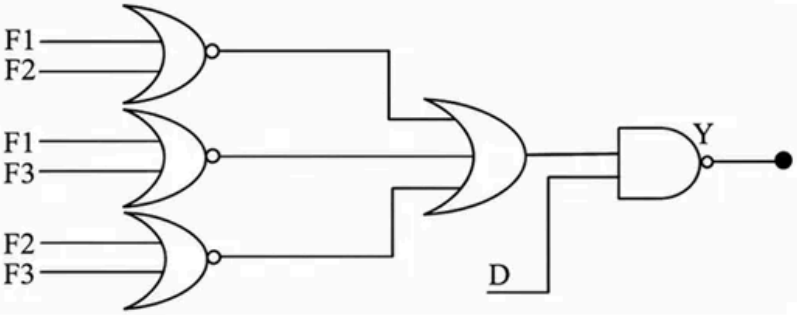
2.



3.



4.

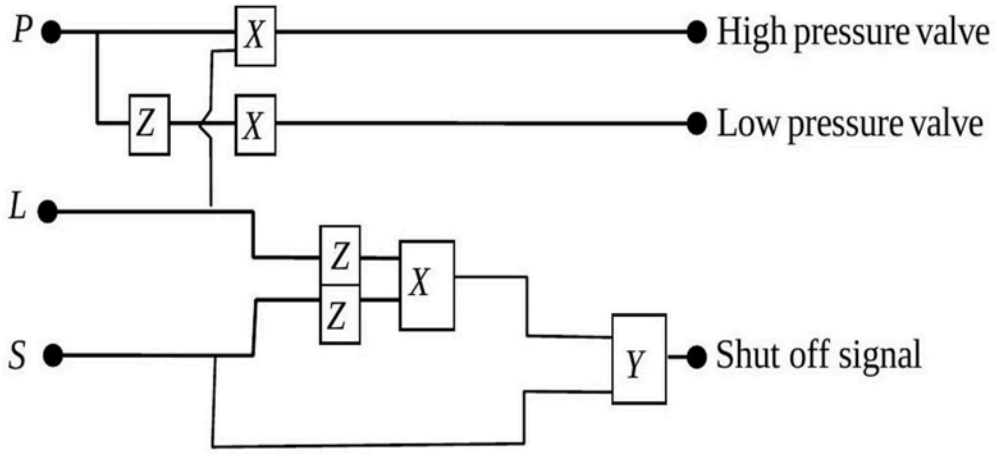


Q9. [June 2022] . 5.0 marks

Electronics > Digital Electronics

CSIR NET	2022 June	5M

A liquid oxygen cylinder system is fitted with a level-sensor (L) and a pressure-sensor (P), as shown in the figure below. The output of L and P are set to logic high ($S = 1$) when the measured values exceed the respective preset threshold values. The system can be shut off either by an operator by setting the input S to high, or when the level of oxygen in the tank falls below the threshold value



The logic gates X, Y and Z , respectively, are

1. OR, AND and NOT
2. AND, OR and NOT
3. NAND, OR and NOT
4. NOR, AND and NOT

Q10. [Dec 2023] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2023 Dec	3.5 M

For three inputs A, B and C , the minimum number of 2 -input NAND gates required to generate the output $Y = \overline{A + B} + \bar{C}$ is

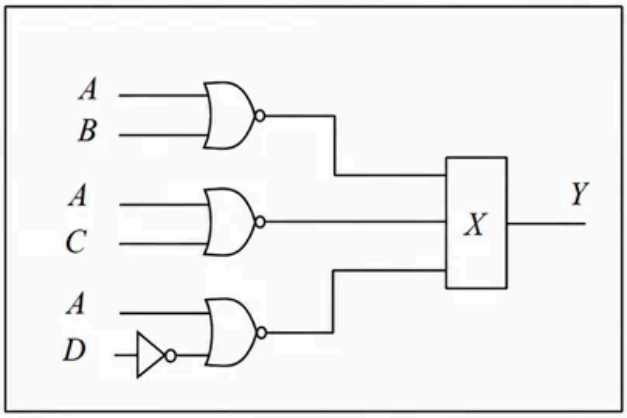
1. 3
2. 4
3. 7
4. 6

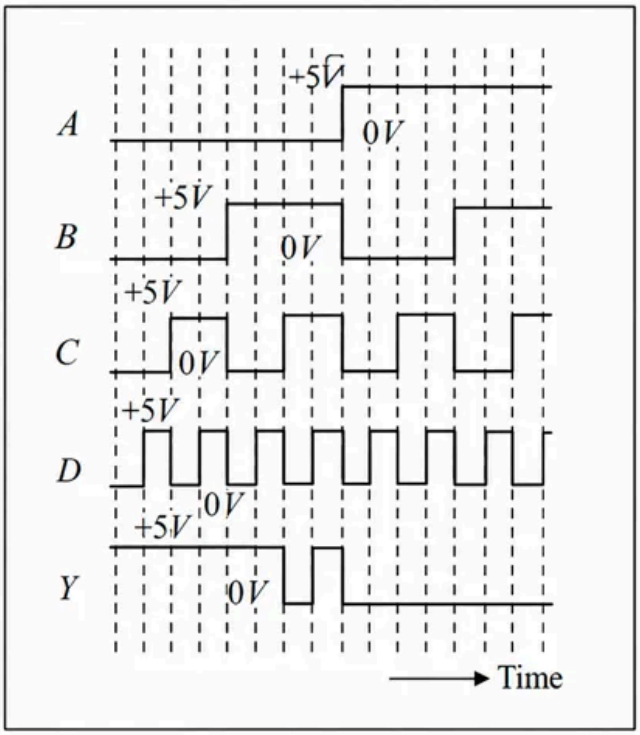
Q11. [June 2023] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2023 June	3.5M

For the given logic circuit, the input waveforms A, B, C and D are shown as a function of time





To obtain the output Y as shown in the figure, the logic gate X should be

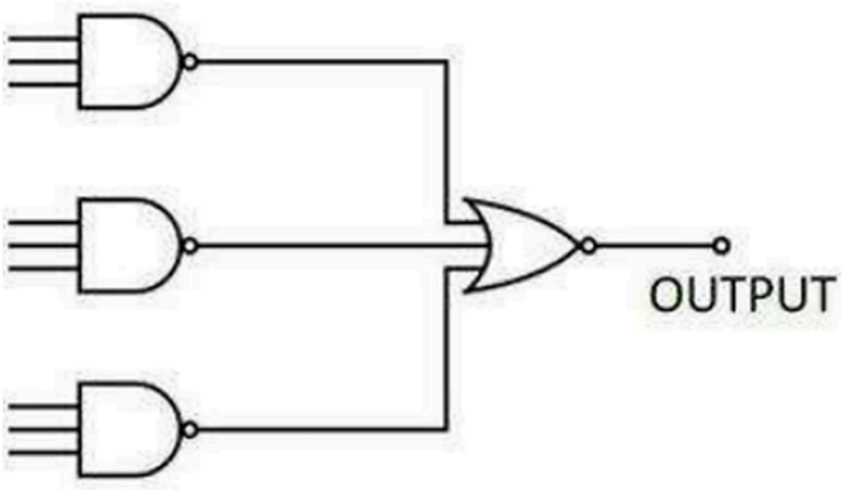
1. an AND gate
2. an OR gate
3. a NAND gate
4. a NOR gate

Q12. [Dec 2024] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2024 Dec	3.5M

The output of the following circuit is always found to be zero.



Such an observation can be due to

1. Two of the inputs of any one of the NAND gates being accidentally shorted to each other
2. One of the inputs to the NOR gate being accidentally grounded
3. One of the inputs to one of the NAND gates being accidentally grounded
4. Two of the inputs of the NOR gate being accidentally shorted to each other

Q13. [Dec 2024] . 5.0 marks

Electronics > Digital Electronics

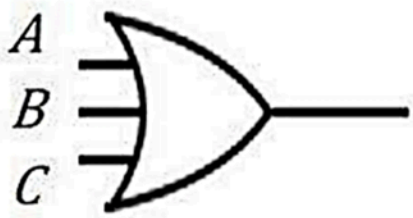
CSIR NET	2024 Dec	5M

The logic circuit that will have the output

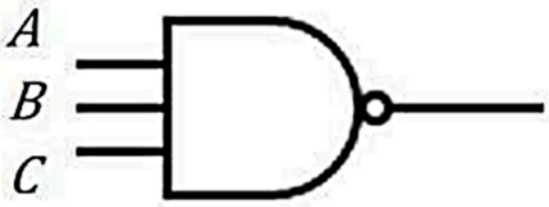
$$Y = (A + B)\overline{(\overline{A}(\overline{B} + \overline{C}))} + \overline{A}(B + C)$$

is

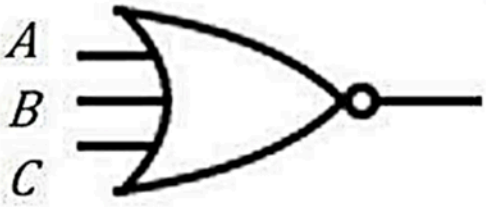
1.



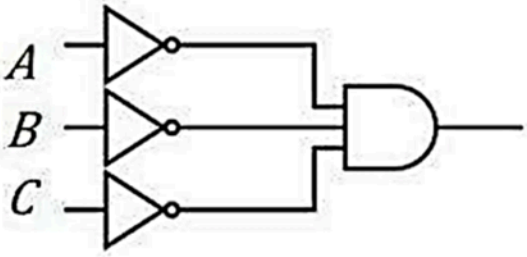
2.



3.



4.



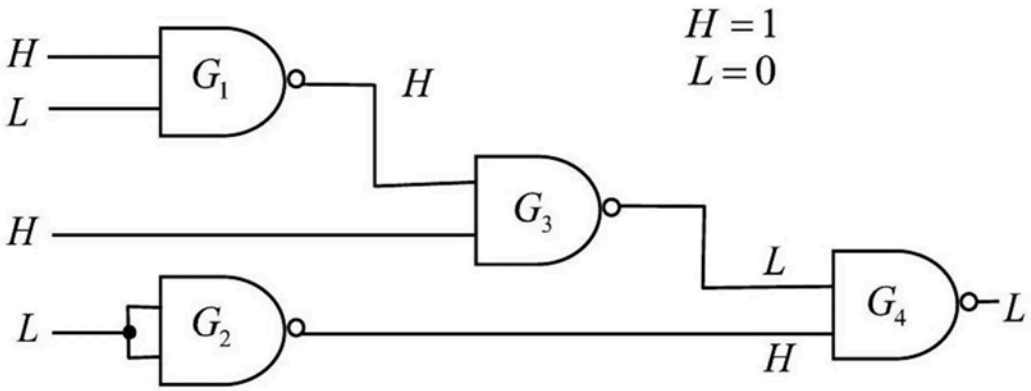
Q14. [June 2024] . 3.5 marks

Electronics > Digital Electronics

CSIR NET	2024 June	3.5M

The logic levels *H* and *L* at different locations in a digital circuit are found to be as shown in the figure. Based on these observations, which of the logic gates is not behaving as an ideal NAND gate?

1. G2
2. G3
3. G4
4. G1



Q15. [Dec 2025] . 5.0 marks

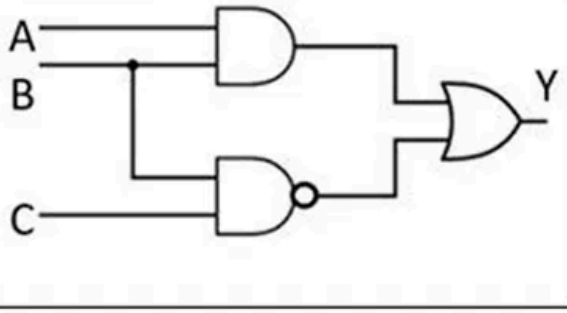
Electronics > Digital Electronics

CSIR NET	2025 Dec	5M	Electronics

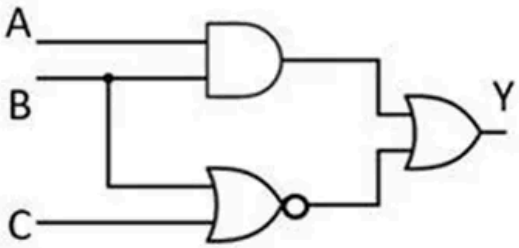
The digital logic circuit that would give the following truth table

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
Y	1	0	0	0	1	0	1	1

1.



2.



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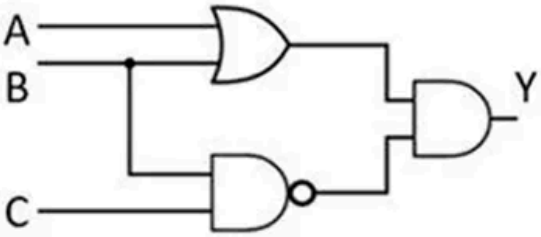
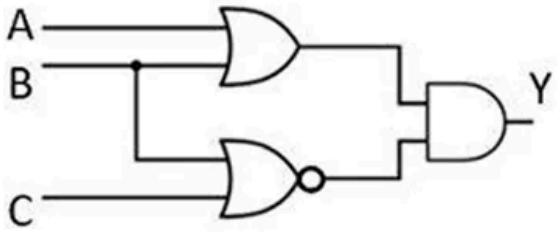


4.



Q16. [June 2025] . 5.0 marks

Electronics > Digital Electronics

CSIR NET	2025 June	5M	Electronics

The minimum number of two input NOR gates required to obtain the following output for three digital inputs A, B and C

$$Y = (\bar{A} + \bar{B} + \bar{C})(\bar{A} + B + \bar{C})(\bar{A} + \bar{B} + C)$$

would be

1. 4
2. 3
3. 5
4. 6

Answer Key

16 questions . Subject and topic for quick revision

Q. No	Subject	Topic	Answer
Q1	Electronics	Digital Electronics	**2&4**
Q2	Electronics	Digital Electronics	**4**
Q3	Electronics	Digital Electronics	**3**
Q4	Electronics	Digital Electronics	**2**
Q5	Electronics	Digital Electronics	**3**
Q6	Electronics	Digital Electronics	**2**
Q7	Electronics	Digital Electronics	**2**
Q8	Electronics	Digital Electronics	**2**
Q9	Electronics	Digital Electronics	**None**
Q10	Electronics	Digital Electronics	**2**
Q11	Electronics	Digital Electronics	**2**
Q12	Electronics	Digital Electronics	**3**
Q13	Electronics	Digital Electronics	**1**
Q14	Electronics	Digital Electronics	**3**
Q15	Electronics	Digital Electronics	**2**
Q16	Electronics	Digital Electronics	**1**

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